1. A lock detection circuit in communication with a phase lock loop to detect phase-frequency lock of an output frequency signal of said phase lock loop with an input reference signal, comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal of said phase lock loop to provide a frequency deviation signal; and

a second logic function circuit to combine the frequency deviation signal with the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said input reference signal and provide an error signal.

2. The lock detection circuit of claim 1 further comprising a latching circuit in communication with the second logic function and the input reference signal to capture and retain said error signal to provide an unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop.

3. The lock detection circuit of claim 1 further comprising an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

4. The lock detection circuit of claim 1 further comprising a frequency divider connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

5. The lock detection circuit of claim 1 wherein the first logic function circuit is an OR gate.

6. The lock detection circuit of claim 1 wherein the second logic function circuit is an AND gate.

7. A lock detection circuit in communication with a phase lock loop to detect phase-frequency lock of an output frequency signal of said phase lock loop with an input reference signal, comprising:

a phase-frequency detector in communication with the phase lock loop to receive the output frequency signal and the input reference signal to generate a frequency increase signal and a frequency decrease signal indicative of an amount of phase-frequency deviation of the output frequency signal has from the input reference signal;

a first logic function circuit connected to the phase frequency detector to combine a frequency increase signal and a

frequency decrease signal to provide a frequency deviation signal; and

a second logic function circuit to combine the frequency deviation signal with the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said input reference signal and provide an error signal.

8. The lock detection circuit of claim 7 wherein the first logic function circuit is an OR gate.

9. The lock detection circuit of claim 7 wherein the second logic function circuit is an AND gate.

10. A phase lock loop system comprising:

a phase-frequency detector to detect a difference in frequency between an output frequency of said phase lock loop and an input reference frequency of said phase lock loop; and

a lock detection circuit to detect loss of phase-frequency lock of the output frequency signal of said phase lock loop with the input reference signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal received from said phase-frequency detector to provide a frequency deviation signal; and

a second logic function circuit to combine the frequency deviation signal with the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said input reference signal and provide said unlock alarm.

11. The phase lock loop of claim 10 wherein the lock detection circuit further comprises a latching circuit in communication with the second logic function and the input reference signal to capture and retain said unlock alarm to provide an unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop.

12. The phase lock loop of claim 10 wherein the lock detection circuit further comprises an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

13. The phase lock loop of claim 10 wherein the lock detection circuit further comprises a frequency divider connected to receive the input reference

signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

14. The phase lock loop of claim 10 wherein the first logic function circuit is an OR gate.

15. The phase lock loop of claim 10 wherein the second logic function circuit is an AND gate.

16. A phase lock loop system comprising:

a lock detection circuit to detect loss of phase-frequency lock of an output frequency signal of said phase lock loop with input reference signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a phase-frequency detector in communication with a voltage controlled oscillator of the phase lock loop to receive the output frequency signal and the input reference signal to generate a frequency increase signal and a frequency decrease signal indicative of an amount of phase-frequency deviation of the output frequency signal has from the input reference signal;

a first logic function circuit connected to the phase frequency detector to combine a frequency increase signal and a frequency decrease signal to provide a frequency deviation signal; and

a second logic function circuit to combine the frequency deviation signal with the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said input reference signal and provide said unlock alarm.

17. The phase lock loop of claim 16 wherein the first logic function circuit is an OR gate.

18. The phase lock loop of claim 16 wherein the second logic function circuit is an AND gate.

19. A clock extraction circuit to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with an reference timing signal extracted from a data stream, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said data stream;

a phase lock loop in communication with the clock extractor to receive said timing signal and adjust a phase and frequency of the local oscillator signal synchronize said local oscillator signal to the timing signal; and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal received from said phase lock loop to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said timing signal and provide said unlock alarm.

20. The clock extractor of claim 19 wherein the lock detection circuit further comprises a latching circuit in communication with the second logic function and the input reference signal to capture and retain said unlock alarm to provide an unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop.

21. The clock extractor of claim 19 wherein the lock detection circuit further comprises an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

22. The clock extractor of claim 19 wherein the lock detection circuit further comprises a frequency divider connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

23. The clock extractor of claim 19 wherein the first logic function circuit is an OR gate.

24. The clock extractor of claim 19 wherein the second logic function circuit is an AND gate.

25. A clock extraction circuit to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with an reference timing signal extracted from a data stream, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said data stream;

a phase lock loop in communication with the clock extractor to receive said timing signal and adjust a phase and frequency of the local oscillator signal synchronize said local oscillator signal to the timing signal; and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a phase-frequency detector in communication with the phase lock loop to receive the output frequency signal and the input reference signal to generate a frequency increase signal and a frequency decrease signal indicative of an amount of phase-frequency deviation of the output frequency signal has from the input reference signal,

a first logic function circuit connected to the phase frequency detector to combine a frequency increase signal and a frequency decrease signal to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater duration than a

portion of a cycle of said timing signal and provide said unlock alarm.

26. The clock extractor of claim 25 wherein the first logic function circuit is an OR gate.

27. The clock extractor of claim 25 wherein the second logic function circuit is an AND gate.

28. A synchronous communication receiver system to receive a synchronous transport signal containing data and an embedded reference timing signal and to extract said data and the reference timing signal, comprising:

a receiver to receive and buffer said synchronous transport signal; and

a clock extraction circuit in communication with the receiver to receive the synchronous transport signal and to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with an reference timing signal extracted from a data stream, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said synchronous transport signal,

a phase lock loop in communication with the clock extractor to receive said reference timing signal and adjust a phase and frequency of the local oscillator signal synchronize said local oscillator signal to the timing signal, and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal received from said phase lock loop to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said timing signal and provide said unlock alarm.

29. The synchronous communication receiver system of claim 28 wherein the lock detection circuit further comprises a latching circuit in communication with the second logic function and the input reference signal to capture

and retain said unlock alarm to provide an unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop.

30. The synchronous communication receiver system of claim 28 wherein the lock detection circuit further comprises an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

31. The synchronous communication receiver system of claim 28 wherein the lock detection circuit further comprises a frequency divider connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

32. The synchronous communication receiver system of claim 28 wherein the first logic function circuit is an OR gate.

33. The synchronous communication receiver system of claim 28 wherein the second logic function circuit is an AND gate.

34. A synchronous communication receiver system to receive a synchronous transport signal containing data and an embedded reference timing signal and to extract said data and the reference timing signal, comprising:

a receiver to receive and buffer said synchronous transport signal; and

a clock extraction circuit in communication with the receiver to receive the synchronous transport signal and to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with an reference timing signal extracted from a data stream, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said synchronous transport signal,

a phase lock loop in communication with the clock extractor to receive said reference timing signal and adjust a phase and frequency of the local oscillator signal synchronize said local oscillator signal to the timing signal, and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a phase-frequency detector in communication with the phase lock loop to receive the output frequency signal and the input reference signal to generate a frequency increase

signal and a frequency decrease signal indicative of an amount of phase-frequency deviation of the output frequency signal has from the input reference signal,

a first logic function circuit connected to the phase frequency detector to combine a frequency increase signal and a frequency decrease signal to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said timing signal and provide said unlock alarm.

35. The clock extractor of claim 34 wherein the first logic function circuit is an OR gate.

36. The clock extractor of claim 34 wherein the second logic function circuit is an AND gate.

37. A synchronous communication system for the transfer of a synchronous transport signal, comprising:

a synchronous transmission apparatus to combine a data signal and a timing reference signal to form the synchronous transport signal; and

a synchronous communication receiver apparatus in communication with the synchronous transmission apparatus to receive the synchronous transport signal band to extract said data and the reference timing signal, comprising:

a receiver to receive and buffer said synchronous transport signal,

a clock extraction circuit in communication with the receiver to receive the synchronous transport signal and to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with the reference timing signal extracted from a synchronous transport signal, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said synchronous transport signal,

a phase lock loop in communication with the clock extractor to receive said reference timing signal and adjust a phase and frequency of the local oscillator signal

synchronize said local oscillator signal to the timing signal, and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal received from said phase lock loop to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said timing signal and provide said unlock alarm.

38. The synchronous communication system of claim 37 wherein the lock detection circuit further comprises a latching circuit in communication with the second logic function and the input reference signal to capture and retain said unlock alarm to provide an unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop.

39. The synchronous communication system of claim 37 wherein the lock detection circuit further comprises an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

40. The synchronous communication system of claim 37 wherein the lock detection circuit further comprises a frequency divider connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

41. The synchronous communication system of claim 37 wherein the first logic function circuit is an OR gate.

42. The synchronous communication system of claim 37 wherein the second logic function circuit is an AND gate.

43. The synchronous communication system of claim 37 wherein said synchronous communication system is a SONET communication system.

44. A synchronous communication system for the transfer of a synchronous transport signal, comprising:

a synchronous transmission apparatus to combine a data signal and a timing reference signal to form the synchronous transport signal;

a synchronous communication receiver apparatus in communication with the synchronous transmission apparatus to receive the synchronous transport signal band to extract said data and the reference timing signal, comprising:

a receiver to receive and buffer said synchronous transport signal,

a clock extraction circuit in communication with the receiver to receive the synchronous transport signal and to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with the reference timing signal extracted from a synchronous transport signal, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said synchronous transport signal,

a phase lock loop in communication with the clock extractor to receive said reference timing signal and adjust a phase and frequency of the local oscillator signal

synchronize said local oscillator signal to the timing signal, and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a phase-frequency detector in communication with the phase lock loop to receive the output frequency signal and the input reference signal to generate a frequency increase signal and a frequency decrease signal indicative of an amount of phase-frequency deviation of the output frequency signal has from the input reference signal,

a first logic function circuit connected to the phase frequency detector to combine a frequency increase signal and a frequency decrease signal to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater

duration than a portion of a cycle of said timing signal and provide said unlock alarm.

45. The synchronous communication system of claim 44 wherein the first logic function circuit is an OR gate.

46. The synchronous communication system of claim 44 wherein the second logic function circuit is an AND gate.

47. The synchronous communication system of claim 44 wherein said synchronous communication system is a SONET communication system.

48. A method for providing an unlock alarm denoting loss of phase frequency synchronism of a phase lock loop comprising the steps of:

providing an input reference timing signal;

providing an increase frequency signal and a decrease frequency signal from said phase lock loop said increase and decrease frequency signals indicating existence of an error in the phase-frequency between an input reference timing signal applied to said phase lock loop and an output local oscillator signal;

performing a first logical combining of said increase frequency signal and said decrease frequency signal to create a phase-frequency deviation signal;

performing a second logical combining of said phase-frequency deviation signal and the input reference timing signal;

if the phase-frequency deviation signal has a greater duration than a portion of a cycle of said timing signal, providing the unlock alarm signal.

49. The method of claim 48 further comprising the step of:

capturing and retaining said unlock alarm signal for transfer to external circuitry.

50. The method of claim 48 further comprising the steps of:

integrating the unlock alarm signal; and

upon said integrated unlock alarm signal surpassing a threshold value transferring externally said unlock alarm signal.

51. The method of claim 48 further comprising the step of:

dividing the input reference timing signal; and

performing the second logical combining the phase-frequency error signal and the divided input reference timing signal.

52. The method of claim 48 wherein the first logical combining is an OR function.

53. The method of claim 48 wherein the second logic logical combining is an AND function.

54. A method for providing an unlock alarm denoting loss of phase frequency synchronism of a phase lock loop comprising the steps of:

providing an input reference timing signal;

providing an output timing signal from said phase lock loop;

detecting a phase-phase frequency deviation between the output timing signal and the input reference timing signal;

if said output timing signal lags or has a lower frequency than said input reference timing signal providing an increase frequency signal;

if said output timing signal leads or has a higher frequency than said input reference timing signal providing a decrease frequency signal;

performing a first logical combining of said increase frequency signal and said decrease frequency signal to create a phase-frequency deviation signal;

performing a second logical combining of said phase-frequency deviation signal and the input reference timing signal;

if the phase-frequency deviation signal has a greater duration than a portion of a cycle of said timing signal, providing the unlock alarm signal.

55. The method of claim 54 wherein the first logical combining is an OR function.

56. The method of claim 54 wherein the second logic logical combining is an AND function.